



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

13 / Suppl.
IDS
E. Willis
3-25-03

Application Serial No. 10/071,456
Filing Date February 8, 2002
Inventor David L. Dickerson et al.
Assignee Micron Technology, Inc.
Group Art Unit 2814
Examiner Ann D. Mai
Attorney's Docket No. MIP-1843
Title: Semiconductor Constructions

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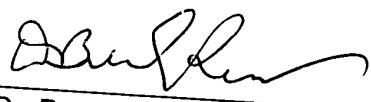
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
References - See Attached Form PTO-1449

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 1-22-03

By: 
D. Brent Kenady
Reg. No. 40,045

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PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
M122-1943SERIAL NO.
10/071,456

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LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
David L. Dickerson et al.FILING DATE
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U.S. PATENT DOCUMENTS

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA					
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FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation	
					Yes	No
AM						
AN						
AO						
AP						
AQ						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

AR		K. Ishimaru et al., <i>Trench Isolation Technology with 1 Micron Depth n-and p-Wells for a Full CMOS SRAM Cell with a 0.4 Micron. . . .</i> IEEE 1994 pps. 97-98
AS		
AT		

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.